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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/900,302	07/06/2001	Rajiv V. Joshi	YOR9-2001-0512US1 (728-21	5687

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EXAMINER
CHO, JAMES HYONCHOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 02/26/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/900,302	JOSHI ET AL.	
	Examiner	Art Unit	
	James H. Cho	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on February 10, 2003 has been entered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2 and 4-9 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Sridhar et al. (US PAT No. 5,528,177).

Regarding claim 1, Fig. 2b and 2g of Sridhar et al. teaches a MOSFET logic circuit (CFET, MOSFET, MOS, PFET, NFET logic are interchangeable; col. 1, lines 14-23) for performing a logic OR operation (Fig. 2g performs an OR/NOR function; col. 11, lines 33-41) comprising three transistors (221, 222, 224), first and second transistors (221, 222) forming a transmission gate (TRANSMISSION GATE in Fig. 2b) outputting one signal (output signal at 231) where at least two input signals (A, B, /A, /B) are

provided to the first and second transistors and an output signal indicative of an OR operation (A+B; the OR output at 231 is further inverted by the inverter 232 and is shown as a NOR function) performed on a first and second input signal (A, B) of the at least two input signals is output from the MOSFET logic circuit.

Regarding claim 2, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where the three transistors include first and second PMOS transistors (222, 224) and one NMOS transistor (221).

Regarding claim 4, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where first input signal (A) is provided to a source of first and second transistors of the three transistors (221, 222), the second input signal (B) is provided to a gate of the second transistor (222), and a complement of the second input signal (/B) is provided to a gate of the first transistor (221).

Regarding claim 5, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where a complement of the second input (/B) is provided to a gate of a third transistor (224) of the three transistors.

Regarding claim 6, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where the at least two input signals to the first and second transistors further comprise a complement of the second input signal (/B).

Regarding claim 7, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where when the second input signal has a logic LOW level the output of the MOSFET logic circuit is an output signal of the transmission gate (when B= logic LOW, 224 is turned off and 222 is turned on so that the output is A).

Regarding claim 8, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where a third transistor (224) of the three transistors is a pull-up transistor (224 pulls up to VCC when turned on) and when the second input signal has a logic high level the output of the MOSFET logic circuit has a voltage level approximately equal to a drain of the third transistor which pulls up the output signal from the transmission gate to a logic HIGH level (when B=high, 224 is turned on and pulls up the output signal at 231).

Regarding claim 9, Fig. 2b and 2g of Sridhar et al. teaches the MOSFET logic circuit as in claim 1 where a delay of the MOSFET logic circuit is one of a delay of a transmission gate formed by first and second transistors of the three transistors, and a delay of a third transistor of the three transistors (delay through 221 and 222 and turn-on delay of 224).

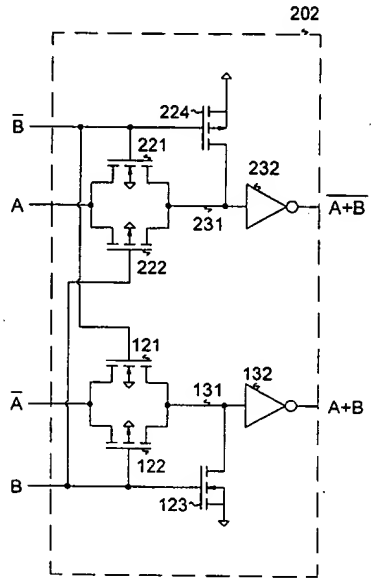
Response to Remarks

3. Applicant's remarks filed December 10, 2002 have been fully considered but they are not deemed to be persuasive regarding claims 1-2 and 4-9.

On page 2 of the amendment, applicant argues that Fig. 2b and 2g of Sridhar et al. does not disclose or suggest a transmission gate formed by first and second transistors of the three transistors outputs one signal and the output signal is OR operation and the output of Fig. 2b. of Sridhar et al. performs an AND operation not an OR operation by citing Col. 10, lines 45-60 and col. 11, line 13-41. The examiner wholly concur the applicant's explanation of Fig. 2b in terms of being used for an AND operation.

However, the examiner notes that the circuit Fig. 2b of Sridhar et al. is used as an AND/NAND operation as shown in Fig. 2f as well as an OR or NOR operation as shown in Fig. 2g. The dual functions of the same circuit is described in Col. 11, lines 29-41, i.e. "This circuit can also be used to implement an OR/NOR function ...Fig. 2g is a schematic diagram illustrating an embodiment of a pair of CFET logic circuit as shown in Figs. 2b and 2d connected as a paired circuit 202 to provide an OR/NOR function". Following truth table for Fig. 2g clearly shows that the output at 231 of Fig. 2g is an OR operation (PMOS 224 and 222 and NMOS 221):

FIG. 2g



A input to 221 and 222	B input to the gate of 222	/B input to the gates of 221 and 224	**Output at 231**	Output of 232
0	0	1	0	1
0	1	0	1	0
1	0	1	1	0
1	1	0	1	0

Therefore, Fig. 2b and Fig. 2g of Sridhar et al. clearly discloses and suggest every element claimed in the independent Claim 1 as well as dependents Claims 2 and 4-9.

Conclusion

4. All claims are drawn to the same invention claimed in the application prior to the entry of the submission under 37 CFR 1.114 and could have been finally rejected on the grounds and art of record in the next Office action if they had been entered in the application prior to entry under 37 CFR 1.114. Accordingly, **THIS ACTION IS MADE FINAL** even though it is a first action after the filing of a request for continued examination and the submission under 37 CFR 1.114. See MPEP § 706.07(b). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James H. Cho whose telephone number is 703-306-5442. The examiner can normally be reached on Monday-Friday, 05:30am-02:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 703-305-3493. The fax phone numbers

for the organization where this application or proceeding is assigned are 703-308-0142 for regular communications and 703-308-0142 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

JHC
February 21, 2003

Michael J. Tokar

Michael Tokar
Supervisory Patent Examiner
Technology Center 2800